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| Day | Chapter | Topic | No. of lecture |
| Day-1 | **Basic Structure of Computers** | Introduction, Computer Types | 1 |
| Day-2 | CA and CO and their relationship,  Von-Neumann Vs Harvard concept | 1 |
| Day-3 | Functional units, Basic operational concepts, Bus Structures and Types | 1 |
| Day-4 | Basic Performance measurement 1 | 1 |
| Day-5 | Basic Performance measurement 2 | 1 |
| Day-6 | **Machine Instructions and Program**s | Memory location and Addressing mechanism | 1 |
| Day-7 | Big- and Little-Endian schemes | 1 |
| Day-8 | Memory operations, Instruction and instruction sequencing | 1 |
| Day-9 | Instruction Format, Instruction length (0,1,2,3 address) with problem 1 | 1 |
| Day-10 | Instruction Format, Instruction length (0,1,2,3 address) with problem 2 | 1 |
| Day-11 | Instruction Format, Instruction length (0,1,2,3 address) with problem 3 | 1 |
| Day-12 | Different CPU organization(GPRS, STACK, ACCUMULATOR) | 1 |
| Day-13 | Addressing modes 1 | 1 |
| Day-14 | Addressing modes 2 | 1 |
| Day-15 | Assembly Language | 1 |
| Day-16 | Basic Input and Output Operations, Subroutines | 1 |
| Day-17 | Additional Instructions (Logic and Shift/Rotate Instructions) |  |
| Day-18 | Tutorial Activity (Quiz/Test/Assignment) | 1 |
| Day-19 | **Basic Processing Unit** | Fundamental concept, Steps taken by CPU | 1 |
| Day-20 | Single bus CPU organization | 1 |
| Day-21 | Control signals required for an instruction  Execution of a complete instruction 1 | 1 |
| Day-22 | Control signals required for an instruction  Execution of a complete instruction 2 | 1 |
| Day-23 | Control signals required for an instruction  Execution of a complete instruction 3 | 1 |
| Day-24 | Multiple bus CPU organization 1 | 1 |
| Day-25 | Multiple bus CPU organization 2 | 1 |
| Day-26 | Design of control unit: Hardwired 1 | 1 |
| Day-27 | Design of control unit: Hardwired 2 | 1 |
| Day-28 | Design of control unit: Micro programmed | 1 |
| Day-29 | Tutorial Activity (Quiz/Test/Assignment) | 1 |
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| Day-30 | Memory Organization | Basic concepts, Memory hierarchy and it’s need, Parameters used to measure the performance. | 1 |
| Day-31 | Types of memory components., Semiconductor RAM memories, Memory Module Design | 1 |
| Day-32 | Cache memories | 1 |
| Day-33 | Mapping functions 1 | 1 |
| Day-34 | Mapping functions 2 | 1 |
| Day-35 | ~~Replacement Algorithms w.r.t Cache (FIFO, LRU and Optimal)~~ | 1 |
| Day-36 | ~~Memory performance consideration, Memory Interleaving~~ | 1 |
| Day-37 | ~~Virtual memory organization and Mapping(TLB)~~ | 2 |
| Day-38 | Tutorial Activity (Quiz/Test/Assignment) | 1 |
| Day-39 | ALU | ~~Design of Adder (n-bit ripple carry adder, carry look ahead adder)~~ | 1 |
| Day-40 | ~~Multiplication of Positive Numbers~~ | 1 |
| Day-41 | Booth Algorithm | 1 |
| Day-42 | ~~Fast Multiplication~~ | 1 |
| Day-43 | Integer Division (Restoring and non-restoring) | 1 |
| Day-44 | IEEE Floating-point Numbers and its Operations (Single and double precision) | 1 |
| Day-45 | Tutorial Activity (Quiz/Test/Assignment) | 1 |
| Day-46 | I/O Organization | Basics of I/O operations | 1 |
| Day-47 | Accessing I/O Devices, Interface | 1 |
| Day-48 | Memory mapped I/O and I/O mapped I/O Programme Control I/O | 1 |
| Day-49 | Interrupts | 1 |
| Day-50 | DMA | 1 |
| Day-51 | ~~Flynn’s Classification (SISD,SIMD,MISD,MIMD)~~ | 1 |
| Day-52 | ~~RISC vs CISC (UNIT 1)~~ | 1 |
|  | TUTORIAL/ACTIVITY (Central) |  |